Amendments to the Claims

1. (currently amended) A dynamic domino circuit~~, said dynamic circuit~~ comprising:

a logic portion adapted for processing logic of said dynamic domino, circuit;

a first dynamic output portion coupled to said logic portion, said first dynamic output portion having a first dynamic node for dynamically holding a first data;

a second dynamic output portion coupled to said logic portion, said second dynamic output portion having a second dynamic node for dynamically holding a second data;

a third dynamic output portion coupled to said logic portion, said third dynamic output portion having a third dynamic node for dynamically holding a third data;

a first and a second transistors having their gates coupled to said first dynamic node, said first transistor having its drain coupled to said second dynamic node, said second transistor having its drain coupled to said third dynamic node;

a third and a fourth transistors having their gates coupled to said second dynamic node, said third transistor having its drain coupled to said first dynamic node, said fourth transistor having its drain coupled to said third dynamic node; and

a fifth and a sixth transistors having their gates coupled to said third dynamic node, said fifth transistor having its drain coupled to said first dynamic node, said sixth transistor having its drain coupled to said second dynamic node.

2. (currently amended) A dynamic adder~~, said dynamic adder~~ comprising ~~:~~ a plurality of dynamic domino circuits as set forth in claim 1 arranged into a plurality of levels, wherein each of said plurality of dynamic circuit implements a thee term carry logic, wherein inversion of any of said three terms at a dynamic circuit is implemented as a function of true terms.

3. (currently amended) The ~~A~~ dynamic adder of claim 2, further ~~multiplexer, said multiplexer~~ comprising:

a multiplexer coupled to a final stage comprising:

(a) a latch built into said multiplexer; and

(b) a first and a second dynamic select inputs to said multiplexer, wherein said multiplexer functions as a latch using said latch when said first and said second dynamic

select inputs are precharged to logic zero, and wherein said multiplexer functions as a multiplexer when said first and said second select inputs are evaluated to their respective logic values.

4. (currently amended) A dynamic adder to generate dynamic logic inversions~~, said dynamic adder~~ comprising:

a dynamic circuit implementing a mutually exclusive circuit to compute ~~indicate~~ a three terms carry logic, wherein the value of each of the three terms carry logic is represented as a dynamic output ~~an inversion of any group of said three terms carry logic at the dynamic circuit is~~ computed ~~implemented~~ as a function of true terms;

wherein the mutually exclusive circuit includes three dynamic output portions representing one for each of the three terms carry logic where each dynamic output portion is coupled to gates of transistors whose drains are coupled to the other dynamic output portions such that the output of a selected dynamic output portion is exclusive of the values of the other dynamic output portions.

5. (currently amended) The dynamic adder of claim 4 ~~30~~, wherein the three terms carry logic is propagate (p), generate (g), and kill (k).

6. (currently amended) The dynamic adder of claim 4 ~~30~~, further comprising additional dynamic circuits arranged in levels to form a carry chain.

7. (currently amended) The dynamic adder of claim 4 ~~30~~, wherein ~~the~~ groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk).

8. (currently amended) The dynamic adder of claim 7 ~~33~~, wherein the groups of said three terms
carry logic are mutually exclusive.

9. (currently amended) The dynamic adder of claim 8 ~~34~~, wherein the inversion is implemented by (~gk)=(gp)+(gg).

10. (currently amended) The dynamic adder of claim 8 ~~34~~, wherein the inversion is implemented by (~gp)=(gg)+(gk).

11. (currently amended) The dynamic adder of claim 8 ~~34~~, wherein the inversion is implemented by (~gg)=(gp)+(gk).

12. (currently amended) A method of implementing dynamic inversions in a carry chain comprising the steps of:

implementing a three terms logic carry chain for dynamic output portions, wherein the three carry signals are generate (g), propagate (p), and kill (k);

computing the (g), (p) and (k) signals as a function of true terms by generating signals such that the output of a selected dynamic output portion is exclusive of the values of the other dynamic output portions

~~inversion of a group of said signals by utilizing a function, wherein said function is a function of true terms~~.

13. (currently amended) The method of claim 12 ~~38~~, wherein groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk) and wherein the function is (~gp)=(gg)+(gk).

14. (currently amended) The method of claim 12 ~~38~~, wherein groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk) and wherein the function is (~gg)=(gp)+(gk).

15. (currently amended) The method of claim 12 ~~38~~, wherein groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk) and wherein the function is (~gk)=(gp)+(gg) ~~(gg)+(gk)~~.

16. (currently amended) The method of claim 12 ~~38~~, wherein groups of said three terms carry logic compromises group propagate (gp), group generate (gg), and group kill (gk) and wherein the groups of the three carry signals, (gg), (gp), and (gk) are mutually exclusive.